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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Terry C. Coughlin Jr.

Application: METHOD, CIRCUIT LIBRARY AND COMPUTER PROGRAM PRODUCT FOR IMPLEMENTING ENHANCED PERFORMANCE AND REDUCED LEAKAGE CURRENT FOR ASIC DESIGNS

Serial No.: 10/760,502

Filing Date: January 20, 2004

Art Unit: 2825

Examiner: Leigh M. Garbowski

Case: ROC920030381US1

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December 19, 2006 — Date of Deposit
Joan Pennington — Signature
Joan Pennington — Name of person signing

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535 North Michigan Avenue
Unit 1804
Chicago, Illinois 60611

Mail Stop **Appeal Brief-Patents**
Honorable Commissioner Of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF TRANSMITTAL

Sir:

An Appeal Brief for Applicants is being submitted herewith. Please charge the Deposit Account No. 09-0465 of International Business Machine Corporation in the amount of **$500.00** for the fee for filing a brief in support of the appeal (37 CFR §41.20(b)(2) fee code 1402).

The Commissioner of Patents and Trademarks is hereby authorized to charge any additional fees or credit any overpayment in connection with the filing of the above-referred to Appeal Brief to the Deposit Account No. 09-0465 of International Business Machine Corporation. A duplicate copy of this transmittal is enclosed.

Respectfully submitted,

By 

Joan Pennington
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Telephone: 312/670-0736
One of the Attorneys for Applicants

Enclosures

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APPEAL BRIEF FOR APPLICANTS

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One of the Attorneys for Applicants

TABLE OF CONTENTS

TABLE OF CITATIONS

TABLE OF OTHER AUTHORITIES

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535 North Michigan Avenue
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Honorable Commissioner Of Patents
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Alexandria, VA 22313-1450

APPEAL BRIEF FOR APPLICANTS

Sir:

This is an appeal of the final rejection of claims 4-10 under 35 U.S.C. §102(b) and claims 1-3 and 7-9 under §103(a) mailed July 17, 2006. For the reasons set forth below, it is submitted that the Board should reverse the final rejection of claims 1-9.

(1) REAL PARTY IN INTEREST

The real party of interest is International Business Machines Corporation.

(2) RELATED APPEALS AND INTERFERENCES

Applicants' attorney knows of no other appeals or interferences that would have a bearing on the Board's decision in the present appeal.

(3) STATUS OF CLAIMS

Claims 4-6 have been finally rejected under 35 U.S.C. § 102(b) and claims 1-3 and 7-9 have been finally rejected under as unpatentable under 35 U.S.C. § 103(a) in an office action mailed July 17, 2006. The rejections of each of the pending claims 1-9 have been appealed.

(4) STATUS OF AMENDMENTS

No Amendment was filed after the final rejection. An advisory action was mailed on November 3, 2006.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

The claimed invention as recited by independent claims 1, 4 and 7 and representative dependant claims 3, 6 and 9 can best be appreciated and understood with reference to the patent specification (hereinafter page p., line l.) and drawings of the invention.

The present invention effectively implements enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs, an alternate voltage threshold (AVT) circuit library and a computer program product for implementing enhanced performance and reduced leakage current for application

specific integrated circuit (ASIC) designs in a computer system, solving a problem of the prior art. (p. 3, l. 10-15, p. 4, l. 16-21, l. 28 - p. 5, l. 8, p. 5 l. 29 - p. 6, l. 2)

Prior art circuit libraries are available in several variations of VTs which can be mixed and matched throughout the chip. Very complex chip methodologies are used to determine where a LVT circuit should be used in place of a Standard VT (SVT) circuit to increase performance. There are hard limits on the number of LVT circuits used on a chip to keep the leakage current under control. The goal is to get the highest performing circuits paths without violating leakage current limits. Using this technique a chip would be laid out using circuits from the SVT library. A timing run would be performed to determining the critical path circuits. Circuits in the critical path would be replaced with the logically equivalent circuits from the LVT library until the maximum number of LVT circuits is used to meet the leakage power requirement. This iterative process can consume many hour of CPU time performing chip layout, RC extraction and timing analysis before a final design is complete. (p. 2. l. 16-29)

Independent claim 1 recites a method for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs comprising the steps of:

identifying standard voltage threshold (SVT) circuits in a circuit library; (p. 6, l. 25-29)

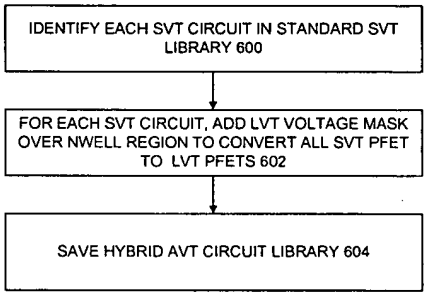
for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid

alternate voltage threshold (AVT) circuit; and (p. 6, l. 29-32)

saving each said AVT circuit in an alternate circuit library. (p. 6, l. 32-34).

As recited in independent claim 1, the method of the invention solves a problem of the prior art implementing application specific integrated circuit (ASIC) designs having high performance and reduced leakage current, see the flowchart of FIG. 6:

FIG. 6



Independent claim 4 recites an alternate voltage threshold (AVT) circuit library comprising:

a plurality of hybrid AVT circuits, (p. 3, l. 10-15, p. 4, l. 16-21)

each said hybrid AVT circuit including (p. 3, l. 10-24)

a plurality of P-channel field effect transistors (PFETs) and a plurality of N-channel field effect transistors (NFETs); (p. 3, l. 10-15, p. 4, l. 16-21, l. 28 - p. 5, l. 8)

each P-channel field effect transistor (PFET) having a low voltage threshold (LVT); and (p. 3, l. 22-24, l. 28-30, p. 5, l. 17-19, p. 5 l. 30 - p. 6, 2)

each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT). (p. 3, l. 22-24, p. 4, l. 29 - p. 5, l. 8, p. 5 l. 27-28).

In accordance with features of the preferred embodiment, the AVT circuit library has been designed that has higher performance as compared to the SVT circuit library without the high leakage of the LVT circuit library. The improved results in performance and leakage current parameters are achieved using the AVT circuit library without the added cost of the AVT mask for processing. In accordance with features of the invention, all the PFETs in the SVT circuit library are replaced with LVT PFETs. Due to the nature of PFETs, PFETs are larger and slower than NFETs in any given CMOS technology. Converting the SVT PFETs to LVT PFETs results in a much faster rise time for any given circuit. The SVT NFET controls the leakage current to ground when the NFET is in the off state. Assuming an even distribution of "1" and "0" states on a chip, the SVT NFET keeps the leakage current to one-half the leakage current that an equivalent LTV circuit would allow. The fall time of the SVT NFET remains the same, but the circuit is more balanced because the faster rise time of the LVT PFETs more closely matches the fall time of SVT NFETs. (p. 4, l. 22- p. 5, l. 8).

Independent claim 7 recites a computer program product for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of: (p. 3, l.10-24, p. 6, l. 13-24)

identifying standard voltage threshold (SVT) circuits in a circuit library; (p. 6, l. 25-29)

for each SVT circuit, replacing each SVT P-channel field effect transistor

(PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and (p. 6, l. 29-32)

saving each said AVT circuit in an alternate circuit library. (p. 6, l. 32-34).

Dependent claim 3 further defines the invention depending from claim 2 which recites that the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET, reciting wherein the step of adding a low voltage threshold (LVT) mask over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET. (p. 5, l. 24-28, p. 5, l. 30 - p. 6, l. 2)

See FIG. 3B, the PFET 302 is a LVT device and the NFET 304 is a SVT device. As shown in FIG. 3B, a low voltage threshold mask or LVT shape is added only over the Nwell Region to convert a SVT PFET to the LTV PFET 302. The PFET 302 is isolated from the NFET 304 and the NFET 304 is maintained as a SVT NFET. Implementation of the AVT circuit library of the invention is very simple due to the nature of standard cell or gate array layouts. All the PFETs in the Nwell Region are isolated from the NFETs. For every circuit in the SVT library, a single shape or low voltage threshold mask is added over the Nwell region to convert the SVT PFETs to LTV PFETs. Once an SVT library is designed, an entire hybrid AVT library can be post-processed in minutes. (p. 5, l. 24 - p. 6. l. 2)

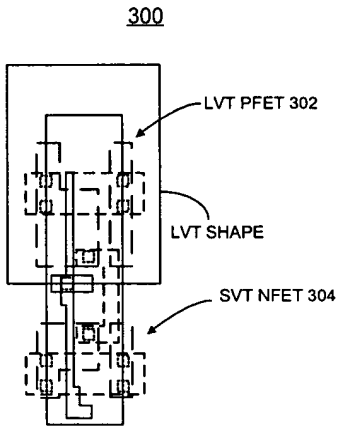


FIG. 3B

Claim 6 further defines the alternate voltage threshold (AVT) circuit library of the invention depending from claim 5 which recites that said hybrid AVT circuits include a corresponding standard voltage threshold (SVT) circuit having a low voltage threshold (LVT) mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET, reciting that wherein each said LVT PFET is provided in an Nwell Region isolated from each said NFET in each said hybrid AVT circuit. (p. 5, l. 24-28)

Claim 9 further defines the computer program product of the invention depending from claim 8 which recites that the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET, reciting that the step of adding a low voltage threshold (LVT) mask over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET. (p. 5, l. 24-28, p. 5, l. 30 - p. 6, l. 2)

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The first ground of rejection presented for review is the rejection of claims 4-6 under 35 USC §102(b) as being anticipated by Chen, U.S. patent 6,078,195.

The second ground of rejection presented for review is the rejection of claims 1-3 and 7-9 under 35 USC §103(a) as being unpatentable over Jones et al., U.S. patent 5,666,288 in view of Chen, U.S. patent 6,078,195.

(7) ARGUMENT

A. INTRODUCTION

The claims 1-9 on appeal do not all stand or fall together. The claims may conveniently be separately considered based upon the recited subject matter. The independent claims at issue here are claims 1, 4, and 7, and representative dependant claims 3, 6, and 9 are separately patentable.

Applicants respectfully submit that the Examiner's rejections under 35 USC §102(b) and under 35 U.S.C. § 103(a) should be reversed because the subject matter of each of the independent claims 1, 4, and 7, and each of the representative dependant claims 3, 6, and 9 is patentable over all the references of record.

Further there is no teaching or suggestion in any of the cited references, individually or taken as a whole, to make the claimed invention obvious.

The rejections of the pending claims under 35 USC §102(b) and under 35 U.S.C. §103(a) are improper and should be reversed.

Applicants respectfully submit that each of the claims 1, 4, and 7, and representative dependant claims 3, 6, and 9, is clearly patentable over all the references of record including Jones et al., and Chen.

Applicants respectfully submit that considering the subject matter as a whole of the claimed invention as recited in each of the independent claims 1, 4, and 7, and representative dependant claims 3, 6, and 9 requires a conclusion that all the claims 1-9 are patentable.

B. THE SCOPE AND CONTENT OF THE PRIOR ART

Chen, U.S. patent 6,078,195

Chen, U.S. patent 6,078,195 discloses logic books with mixed low Vt and regular Vt devices provide a performance gain without the large increase in stand-by power of the logic book. Low Vt devices are used to gain speed, and regular Vt devices are used to cut off the off-current of the logic book. The optimization of mixed Vt configurations is important. No single path between an output and ground can be made of all low Vt devices, and no single path between the output and Vdd can be made of all low Vt devices. Generally, devices that are connected to Vdd and ground should be regular Vt devices, a low Vt devices should be connected closest to the output. All low Vt devices should be appropriately reversely biased in their off states. Because its merits in standby power, speed and noise margin, such mixed-low-and-regular-Vt logic books can have a wide use in VLSI designs (e.g., high performance microprocessor design). Stated at column 4, lines 6-17:

> Of course, there are many possible variations as to how to place, where to place low V_t, and to place how many low V_t devices in a mixed V_t logic book in general. For example, one possible configuration is to have a low V_t NFET, as shown in FIG. 3, where the source of the low V_t device is connected to ground, and another possible configuration is to have both a low V_t NFET device and a low V_t PFET device. They are just trivial extensions of the same basic idea. As our optimization algorithm will show later, these configurations are inferior to the configuration shown in FIG. 2 in terms of gaining speed and minimizing leakage current.
>
> Stated at column 4, lines 35-38: Note that in this circuit NFETs 42 and 46 and PFETs 43 and 44, which are closest to the output, are low V_t devices. NFETs 41 and 45, closest to ground, and PFETs 47 and 48, closest to V_{dd}, are regular V_t devices.
>
> Stated at column 4, lines 49-52: The AND function is made in combination with NFET 55 and PFET 56. In this case, PFET 53 and NFET 55, which are closest to the outputs, are low V_t devices. NFETs 51 and 52, closest to ground, and PFETs 54 and 56, closest to V_{dd}, are regular V_t devices.

Stated at column 4, lines 21-23: In the mixed V_t logic book, it appears that there is a degree of freedom as to which devices should be made low V_t and which should remain regular V_t.

Stated at column 6, lines 22-35: It is also possible to design a mixed V_t book for an inverter, but it is a little trickier. Since there are only two devices in this logic book. The choices are limited to making either the PFET or the NFET the low V_t device, but both cannot be low V_t devices. Another subtle consideration stems from where and how such an inverter is used in circuit. Normally such mixed V_t configuration would give some advantage in lowering the standby power. However, if the output/input is asserted to one particular polarity, care has to be exercised to determine if a low V_t NFET device or low V_t PFET device should be used. All of these considerations can be made into a library or database of a computer program.

Stated at column 11, lines 2-18: In both dynamic type and the static type, the parasitic capacitance has very large impact on speed. Good layout not only saves silicon real estate but also minimizes parasitics. Layout concerns for the mixed V_t is briefly described below. First of all, no new masks are involved in this mixed V_t approach. It uses exactly the same hardware technology as the low V_t book approach that has been implemented in current technology. A separated channel implant is used for making low V_t devices. The same HALO as in regular V_t devices is implanted in the low V_t device to make sure that the low V_t devices have no worse short channel effects than the regular V_t devices. Careful alignment of the low V_t mask to other masks are crucial for the success of making chips containing mixed low V_t and regular V_t devices in a single logic unit. The current ground rules favors use of multi-finger type of mixed V_t layout and have limitation on stacked devices. But this can be changed as the technology evolves.

Jones et al., U.S. patent 5,666,288

Jones et al., U.S. patent 5,666,288 discloses a method and apparatus for designing and manufacturing integrated circuits (ICs) that involves providing an initial library of IC cells (106) and a behavioral circuit model (100) in order to create a gate schematic netlist (102). The gate schematic netlist (102) is optimized by changing individual transistor sizes, power rail sizes, cell pitch, and the like in a step (103). Once the optimization has occurred, the initial library can no longer be used to place and route the IC. Therefore, a hybrid logic cell library is created from the gate schematic

netlist (102) via a step (105). This hybrid library and the above optimizations provide a placed and routed IC via a step (126) in a short design cycle while optimizing performance of the IC.

C. THE REJECTION OF CLAIMS 4-6 AS BEING ANTICIPATED BY CHEN SHOULD BE REVERSED

Anticipation is a question of fact. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). The inquiry as to whether a reference anticipates a claim must focus on what subject matter is encompassed by the claim and what subject matter is described by the reference. As set forth by the court in Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 (1984), it is only necessary for the claims to "'read on' something disclosed in the reference, i.e., all limitations in the claim are found in the reference, or 'fully met' by it." Anticipation under § 102 can be found only when the reference discloses exactly what is claimed; where there are differences between the reference disclosure and the claim, the rejection must be based on § 103 which takes differences into account. Tyler Refrigeration v. Kysor Industrial Corp., 777 F.2d 687, 689, 227 U.S.P.Q. 845 846-47 (Fed. Cir. 1985). It must be shown that the reference contains all of the elements of the claims, and that the elements are arranged in the same way to achieve the same result which is asserted to be an inventive function.

Independent claim 4 is patentable

Independent claim 4 recites an alternate voltage threshold (AVT) circuit library comprising: a plurality of hybrid AVT circuits, each said hybrid AVT circuit including a

plurality of P-channel field effect transistors (PFETs) and a plurality of N-channel field effect transistors (NFETs); each P-channel field effect transistor (PFET) having a low voltage threshold (LVT); and each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT).

Applicants respectfully submit that subject matter of the invention, as recited in independent claim 4, is not anticipated by Chen. The scope and content of the prior art including Chen is believed to be accurately described above. Only Applicants teach an alternate voltage threshold (AVT) circuit library as recited in claim 4.

In accordance with features of the invention, only Applicants teach an alternate voltage threshold (AVT) circuit library including a plurality of PFETs and a plurality of NFETs, each PFET having a low voltage threshold LVT, and each NFET having a standard voltage threshold SVT. The claimed features of the invention are not disclosed, nor remotely suggested in the Chen patent. Chen does not disclose, expressly or under principles of inherency, each and every element of a claimed invention as recited in claim 4. The rejection of claim 4 under 35 U.S.C. § 102(b) is improper and should be reversed.

There are significant differences between what is disclosed in the Chen patent and the pending claims 4-6; and the Examiner's rejection under 35 U.S.C. §102 should be reversed because it is axiomatic that for prior art to anticipate under §102 it has to meet every element of the claimed invention (Hybritech Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1379, 231 USPQ 81, 90 (Fed. Cir. 1986).

Chen teaches an inverter circuit that can include one PFET that is a LVT device

and one NFET that is a SVT device. Contrary to the Examiner's assertion, the inverter circuit of Chen is not equivalent to and does not suggest, an alternate voltage threshold (AVT) circuit library as recited in independent claim 4. It is the claimed invention as recited in independent claim 4 that must be considered in determining anticipation under 35 U.S.C. §102, not a portion of the specification.

An invention is anticipated if it "was . . . described in a printed publication in this. . . country . . . more than one year prior to the date of application for patent in the United States." 35 U.S.C. § 102(b) (2000). A reference must enable someone to practice the invention in order to anticipate under § 102(b), a non-enabling reference may qualify as prior art for the purpose of determining obviousness under § 103. A patent claim is invalid as anticipated if every limitation in a claim is found in a single prior art reference, either explicitly or inherently. See International Corp. V. Milgraum, 192 F.3d 1362, 1365 (Fed. Cir. 1999) "Anticipation is a factual matter, which we review under the clearly erroneous standard." Glaxo v. Novopharm, 52 F.3d 1043, 1047 (Fed. Cir. 1995).

It is well settled that prior art under 35 U.S.C. § 102(b) must sufficiently describe the claimed invention to have placed the public in possession of it. Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention. Accordingly, even if the claimed invention is disclosed in a printed publication, that disclosure will not suffice as prior art if it is not enabling. It is not, however, necessary that an invention disclosed in a publication shall have actually been made in order to

satisfy the enablement requirement. Elan Pharmaceuticals Inc. v. Mayo Foundation, 346 F.3d 1051 (Fed. Cir. 2003).

Chen does not teach, nor suggest, an alternate voltage threshold (AVT) circuit library each said hybrid AVT circuit including a plurality of P-channel field effect transistors (PFETs) and a plurality of N-channel field effect transistors (NFETs). Chen does not teach, nor suggest, such an alternate voltage threshold (AVT) circuit library each said hybrid AVT circuit including each P-channel field effect transistor (PFET) having a low voltage threshold (LVT). Chen does not teach, nor suggest, such an alternate voltage threshold (AVT) circuit library with each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT).

Applicants respectfully submit that Chen does not enable, nor provide any suggestion of an alternate voltage threshold (AVT) circuit library, as taught and claimed by Applicants. A patent claim is invalid as anticipated if every limitation in a claim is found in a single prior art reference, either explicitly or inherently. Smithkline Beecham Corp.v. Apotex Corp., 403 F.3d 1331 (Fed. Cir. 2005). In the disclosed inverter circuit, Chen does not disclose or suggest the limitation of independent claim 4 that each said hybrid AVT circuit including a plurality of P-channel field effect transistors (PFETs) and a plurality of N-channel field effect transistors (NFETs).

Thus, independent claim 4 is patentable.

Dependent claim 6 is patentable

Dependent claim 6 is patentable for the same reasons discussed above relative to claim 4, and is submitted to be separately patentable.

Claim 6 is submitted to be separately patentable because claim 6 further defines that said hybrid AVT circuits include a corresponding standard voltage threshold (SVT) circuit having a low voltage threshold (LVT) mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET; and each said LVT PFET is provided in an Nwell Region isolated from each said NFET in each said hybrid AVT circuit.

Chen does not disclose, nor enable, nor provide any suggestion of a hybrid AVT circuits include a corresponding standard voltage threshold (SVT) circuit having a low voltage threshold (LVT) mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET; and Chen does not disclose, nor enable, nor provide any suggestion of each said LVT PFET is provided in an Nwell Region isolated from each said NFET in each said hybrid AVT circuit. Chen does not anticipate claim 6.

Thus, claim 6 is patentable.

D. THE REJECTION OF CLAIMS 1-3 AND 7-9 AS BEING UNPATENTABLE OVER JONES et al., AND CHEN SHOULD BE REVERSED

The Board should reverse the rejection of claims 1-3 and 7-9 under 35 USC §103 as being unpatentable over Jones et al., U.S. patent 5,666,288 in view of Chen, U.S. patent 6,078,195.

35 U.S.C. §103 requires that the invention as claimed be considered "as a whole" when considering whether the invention would have been obvious when it was made. Graham v. John Deere, 383 U.S. 1, 148 USPQ 459, 472 (1966). It is applicants' claimed invention which must be considered as a whole pursuant to 35 U.S.C. §103,

and failure to consider the claimed invention as a whole is an error of law. In order for there to be a prima facie showing of obviousness under 35 U.S.C. §103, it is necessary that the references being combined in an attempt to demonstrate prima facie obviousness must themselves suggest the proposed combination. For a combination of prior art references to render an invention obvious, "[t]here must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination." In re Oetiker, 977 F.2d 1443, 1447, 24 USPQ2D 1443, 1446 (Fed. Cir. 1992). That one must point to some reason, suggestion, or motivation to make a combination is not to say that the teaching must be explicit, but in order to render an invention obvious by the combination of prior art references, the prior art must contain some reason, suggestion, or motivation. It is impermissible to use the inventor's disclosure as a "road map" for selecting and combining prior art disclosures. In Interconnect Planning Corp. v. Feil 774 F.2d 1132, 1143, 227 USPQ 542, 551 (Fed. Cir. 1985), the Federal Circuit noted that "The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."

Independent claim 1 is patentable

Independent claim 1 recites a method for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs comprising the steps of: identifying standard voltage threshold (SVT) circuits in a circuit library; for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect

transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library.

In accordance with features of the present invention, all the PFETs in the SVT circuit library are replaced with LVT PFETs, as recited in independent claim 1. Due to the nature of PFETs, PFETs are larger and slower than NFETs in any given CMOS technology. Converting the SVT PFETs to LVT PFETs results in a much faster rise time for any given circuit. The SVT NFET controls the leakage current to ground when the NFET is in the off state. Assuming an even distribution of "1" and "0" states on a chip, the SVT NFET keeps the leakage current to one-half the leakage current that an equivalent LTV circuit would allow. The fall time of the SVT NFET remains the same, but the circuit is more balanced because the faster rise time of the LVT PFETs more closely matches the fall time of SVT NFETs.

Applicants respectfully submit that the subject matter of the invention, as recited in independent claim 1 is not rendered obvious from the total teaching of Jones et al. and Chen.

Only Applicants teach each of the steps: for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library.

Applicants respectfully submit that the prior art descriptions of Chen and Jones et al. falls short of applicant's invention, and the subject matter of the claimed invention as recited in claim 1 would not have been obvious to one of ordinary skill in the art in view of the references of record. Further in the cited references, there is no hint of for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library, as taught and claimed by Applicants.

The prior art of record, including the Jones et al. patent and the Chen patent provides no teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art to achieve the claimed invention. 35 U.S.C. § 103 requires that the invention as claimed be considered "as a whole" when considering whether the invention would have been obvious when it was made. Graham v. John Deere, 383 U.S. 1, 148 USPQ 459, 472 (1966). It is applicant's claimed invention which must be considered as a whole pursuant to 35 U.S.C. § 103, and failure to consider the claimed invention as a whole is an error of law.

In the words of the Court of Appeals for the Federal Circuit, "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re John R. Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780 (Fed. Cir.

1992). See In re Gordon and Sutherland, 733 F.2d 900, 221 USPQ 1125, 1127 (Fed. Cir. 1984), Carl Schenck, A.G. v. Nortron Corp., 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983), and In re Sernaker, 702 F.2d 989, 995-96, 217 USPQ 1, 6-7 (Fed. Cir. 1983).

A combination of all the teachings of the references of record would not achieve the claimed invention as recited by claim 1. These steps are not suggested from the total teaching of Jones et al. and Chen. The prior art of record, including Jones et al. and Chen, provides no teaching, suggestion or inference in the prior art as a whole or knowledge generally available to one having ordinary skill in the art to achieve the claimed invention.

Thus, independent claim 1 is patentable.

Independent claim 7 is patentable

Independent claim 7 is submitted to be patentable for the same reasons set forth above in connection with claim 1.

Independent claim 7 recites a computer program product for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of: identifying standard voltage threshold (SVT) circuits in a circuit library; for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor

(NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library.

In order for there to be a prima facie showing of obviousness under 35 U.S.C. §103, it is necessary that the references being combined in an attempt to demonstrate prima facie obviousness must themselves suggest the proposed combination. It is insufficient to establish obviousness that the separate elements of the invention existed in the prior art, absent some teaching or suggestion, in the prior art, to combine the elements. Arkie Lures, Inc. v. Gene Larew Tackle, Inc., 119 F.3d 953, 957, 43 USPQ2d 1294, 1297 (Fed. Cir. 1997).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved. In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). Hindsight in impermissible when an examiner rejects an application in reliance upon teachings not drawn from any prior art disclosure, but from the applicant's own disclosure. In re Dembiczak, 175 F.3d 994, 998, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999). Broad conclusory statements standing alone are not "evidence." Id.

The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. See In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). The mere fact that the prior art could be modified so as to result in the combination defined by the claims would not have made the modification obvious unless the prior art suggests the

desirability of the modification. See In re Gordon and Sutherland, 733 F.2d 900, 221 USPQ 1125, 1127 (Fed. Cir. 1984), Carl Schenck, A.G. v. Nortron Corp., 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983), and In re Sernaker, 702 F.2d 989, 995-96, 217 USPQ 1, 6-7 (Fed. Cir. 1983).

In a proper obviousness determination, "whether the changes from the prior art are 'minor', . . . the changes must be evaluated in terms of the whole invention, including whether the prior art provides any teaching or suggestion to one of ordinary skill in the art to make the changes that would produce the patentee's . . . device." Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 935, 15 USPQ2d 1321, 1324 (Fed. Cir.), cert. denied, 498 U.S. 920, 111 S.Ct. 296, 112 L.Ed.2d 250 (1990). This includes what could be characterized as simple changes, as in In re Gordon and Sutherland, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1983) (Although a prior art device could have been turned upside down, that did not make the modification obvious unless the prior art fairly suggested the desirability of turning the device upside down.). In re Chu, 66 F.3d 292, 298, 36 USPQ2d 1089 (Fed. Cir. 1995).

In Re Fritch, 972 F.2d at 1266, 23 USPQ2d at 1780 (Fed. Cir. 1992), states: "[I]t is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. ... This court has previously stated that '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."

Applicants respectfully submit that the subject matter of the invention, as recited

in independent claim 7 is not rendered obvious from the total teaching of Jones et al. and Chen.

Applicants acknowledge that AVT logic books are known and that a LVT PFET is known. However, prior art arrangements such as disclosed by Jones et al. and Chen fail to achieve the invention, as recited in independent claim 7.

Known complex chip methodologies used to determine where a LVT circuit should be used in place of a Standard VT (SVT) circuit to increase performance require timing runs to be performed in determining the critical path circuits and can consume many hour of CPU time performing chip layout, RC extraction and timing analysis before a final design is complete. In the present invention, all the PFETs in the SVT circuit library are replaced with LVT PFETs, and the SVT NFETs are maintained. Once an SVT library is designed, an entire hybrid AVT library can be post-processed in minutes in accordance with the invention.

Only Applicants teach each of the steps: for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and saving each said AVT circuit in an alternate circuit library.

Thus, independent claim 7 clearly is patentable.

Dependent claim 3 is patentable

Dependent claim 3 is patentable for the same reasons discussed above relative to claim 1, and is submitted to be separately patentable.

Applicants submit that the subject matter of the claimed invention as recited in claim 3 would not have been obvious to one of ordinary skill in the art in view of the references of record. No hint is found in the references of record and the references of record do not suggest the subject matter of the invention as taught and claimed by Applicants in claim 3.

Claim 3 is submitted to be separately patentable because claim 3 further defines that the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET and that adding a low voltage threshold (LVT) mask over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET.

Applicant respectfully submits that the prior art descriptions of Jones et al. and Chen fall short of applicant's invention, and the subject matter of the claimed invention as recited in claim 3 would not have been obvious to one of ordinary skill in the art in view of the references of record. In the cited Jones et al. and Chen references, there is no hint of adding a low voltage threshold (LVT) mask over each said SVT PFET, nor of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET, as taught and claimed by Applicants. A combination of all the teachings of the references of record would not achieve the claimed invention as recited by claim 3.

Thus, dependent claim 3 is patentable.

Dependent claim 9 is patentable

Dependent claim 9 is separately patentable further defining the computer program product of the invention as recited in independent claim 7. Claim 9 is submitted to be separately patentable because claim 9 further defines that the replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET, which includes adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET.

The claimed feature of the computer program product is not shown nor suggested in total combination of the references of record, including Jones et al. and Chen. Thus, claim 9 is patentable over the references of record.

Rejections based on § 103 must rest on a factual basis with these facts being interpreted without hindsight reconstruction of the invention from the prior art. The Examiner may not, because of doubt that the invention is patentable, resort to speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis for the rejection. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968).

Hindsight in impermissible when an examiner rejects an application in reliance upon teachings not drawn from any prior art disclosure, but from the applicant's own disclosure. In re Demiski, 796 F.2d 236,443, 230 USPQ2d 313, 316 (Fed. Cir. 1986); W.L. Gore & Assocs. Inc. V. Garlock, Inc., 721 F.2d 1540, 1553, 220 USP1 303, 313 (Fed. Cir. 1984), cert. Denied, 469 U.S. 851 (1984).

That one must point to some reason, suggestion, or motivation to make a

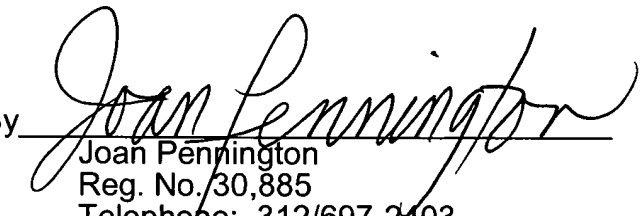
combination is not to say that the teaching must be explicit, but in order to render an invention obvious by the combination of prior art references, the prior art must contain some reason, suggestion, or motivation. It is impermissible to use the inventor's disclosure as a "road map" for selecting and combining prior art disclosures. In Interconnect Planning Corp. v. Feil 774 F.2d 1132, 1143, 227 USPQ 542, 551 (Fed. Cir. 1985), the Federal Circuit noted that "The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."

E. CONCLUSION

Claims 1-9 are patentable over all the references of record and are neither anticipated by Chen, not rendered obvious by the cited combinations Jones et al. and Chen. Each of the claims 1-9 is patentable and the Examiner's rejections should be reversed.

It is respectfully requested that the final rejection be reversed.

Respectfully submitted,

By 

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(8) CLAIMS APPENDIX

CLAIMS ON APPEAL

1. A method for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs comprising the steps of:

identifying standard voltage threshold (SVT) circuits in a circuit library;

for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and

saving each said AVT circuit in an alternate circuit library.

2. A method for implementing enhanced performance and reduced leakage current as recited in claim 1 wherein the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET.

3. A method for implementing enhanced performance and reduced leakage current as recited in claim 2 wherein the step of adding a low voltage threshold (LVT) mask over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET.

4. An alternate voltage threshold (AVT) circuit library comprising:

a plurality of hybrid AVT circuits, each said hybrid AVT circuit including

a plurality of P-channel field effect transistors (PFETs) and a plurality of N-channel field effect transistors (NFETs);

each P-channel field effect transistor (PFET) having a low voltage threshold (LVT); and

each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT).

5. An alternate voltage threshold (AVT) circuit library as recited in claim 4 wherein said hybrid AVT circuits include a corresponding standard voltage threshold (SVT) circuit having a low voltage threshold (LVT) mask added over each said SVT PFET to convert each said SVT PFET to said LVT PFET.

6. An alternate voltage threshold (AVT) circuit library as recited in claim 4 wherein each said LVT PFET is provided in an Nwell Region isolated from each said NFET in each said hybrid AVT circuit.

7. A computer program product for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of:

identifying standard voltage threshold (SVT) circuits in a circuit library;

for each SVT circuit, replacing each SVT P-channel field effect transistor (PFET) with a low voltage threshold (LVT) PFET and maintaining each N-channel field effect transistor (NFET) having a standard voltage threshold (SVT) to provide a hybrid alternate voltage threshold (AVT) circuit; and

saving each said AVT circuit in an alternate circuit library.

8. A computer program product as recited in claim 7 wherein the step of replacing each SVT PFET with a low voltage threshold (LVT) PFET includes the step of adding a low voltage threshold (LVT) mask over each said SVT PFET.

9. A computer program product as recited in claim 8 wherein the step of adding a low voltage threshold (LVT) mask over each said SVT PFET includes the step of adding a single shape defining said low voltage threshold mask over an Nwell region to convert each said SVT PFET to said LTV PFET.

(9) EVIDENCE APPENDIX

None.

(10) RELATED PROCEEDINGS APPENDIX

None.